

SolariaPCB

Dave Rosato Harley Thermal LLC





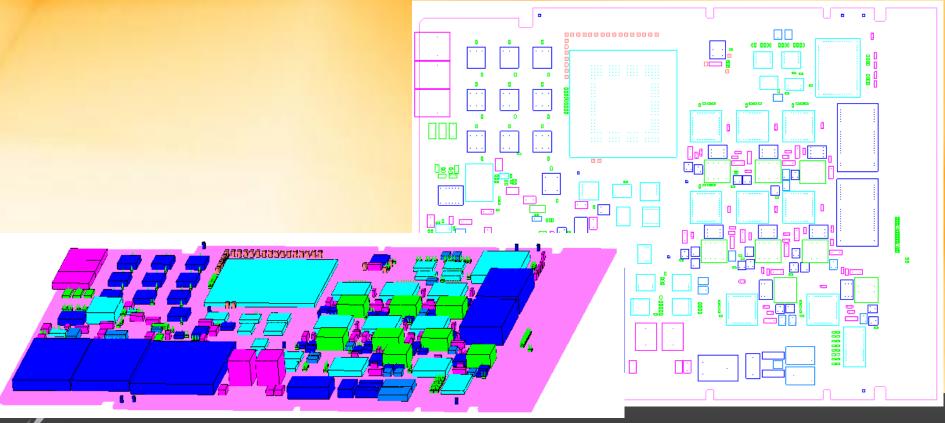
- SolariaPCB imports Electrical CAD data through ODB++ files.
- One compressed file is read and automatically expanded into the folder structure.
- Folders with Layers, Drills (defining vias) and components are identified.

ODB++ Im	port
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Compressed ODB++ File		Import
	Browse	Cancel
Root folder for ODB++ files		
C:\Solaria\SolariaPCB\ODB++\test\ODB	Browse	
5 Layer files,10 Drill files,2 Component files		
ayer Files		
WIR1 WIR2 WIR3 WIR4 WIR5 WIR6		
)rill Files		
WIR1-WIR3WIR1WIR3 WIR1-WIR2WIR1WIR2 WIR3-WIR4WIR3WIR4 WIR4-WIR5WIR4WIR5 WIR1-WIR6SYMBOL-ASYMBOL-B WIR4-WIR6WIR4WIR6		E
Component Files		

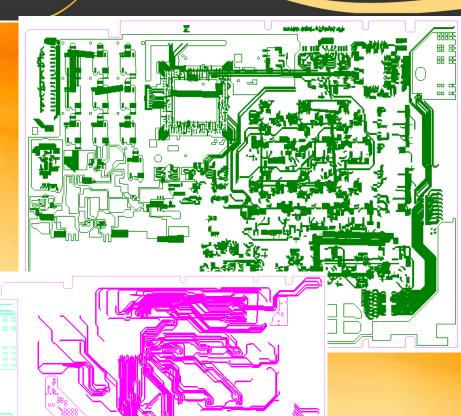


• All components on both sides of the board are imported.



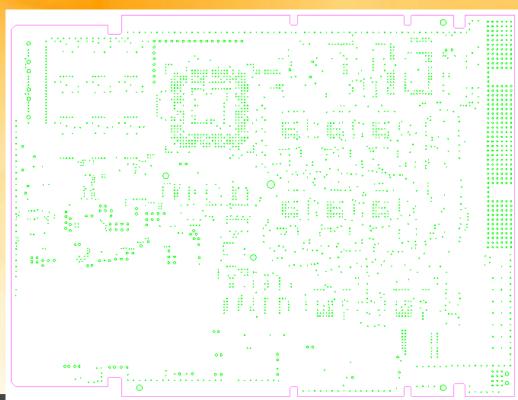


- Every trace on every layer is imported.
- Traces and power and ground planes are the primary lateral heat transfer path.





- Every via between every layer is imported.
- The diameter of each via is imported.
- Vias provide the major heat transfer path through the board thickness.







Board Layers

- Every layer and thickness is imported.
- If ECAD data was not imported, the Coverage checkbox can be checked and a Percentage of metal can be defined. A smearing method is then used to represent the metal for this layer.
- Layers can be manually added. This would be like a metal frame.

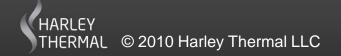
PCB Layers									
	#	Name	Thickness	Туре	Material	Coverage	Percentage	Color	Default Layer Material OK
	1	TOP	1.3999999	Conducting	Copper		0		Cancel
	2	Dielectric 1	.0038504	Dielectric	FR-4 EPOXY/GLASS		0		Conducting
	3	L7	1.3999999	Conducting	Copper		0		C Dielectric Help
	4	Dielectric 3	.004	Dielectric	FR-4 EPOXY/GLASS		0		
	5	L6	1.3999999	Conducting	Copper		0		Conducting material
	6	Dielectric 5	.0034803	Dielectric	FR-4 EPOXY/GLASS		0		Copper 👻 Add Layer
	7	L5	1.3999999	Conducting	Copper		0		
	8	Dielectric 7	.028	Dielectric	FR-4 EPOXY/GLASS		0		Conducting thickness Delete Layer
	9	L4	1.3999999	Conducting	Copper		0		0.0014
	10	Dielectric 9	.0035984	Dielectric	FR-4 EPOXY/GLASS		0		Dielectric material
	11	L3	1.3999999	Conducting	Copper		0		
	12	Dielectric 11	.004	Dielectric	FR-4 EPOXY/GLASS		0		FR-4 EPOXY/GLA 👻
	13	L2	1.3999999	Conducting	Copper		0		Dielectric thickness
	14	Dielectric 13	.0038504	Dielectric	FR-4 EPOXY/GLASS		0		0.005
	15	BOTTOM	1.3999999	Conducting	Copper		0		,
	16	Plate	.005	3D Layer	FR-4 EPOXY/GLASS		100		



Mapping Components to the included library

 This is used to map imported components to those in the SolariaPCB library.

10 PIN HDR	1DDE005256_2	
1K RES	2N7000	ок
220UF_CAP_16V	5DD	Мар
40_PIN_HDR 4 PIN_PWR_CON	69877011 BGA100PCD.04	
560_RES	BGA100PCD.05	Help
68060_PGA 74ALS08	BGA100PCD.06 BGA100PCU.04	
EPM7256S_7	BGA100PCU.05	Cancel
FUSE_HOLDER	BGA100PHDCD.05	
GRN_ORG_LED	BGA100PHDCU.05 BGA100PLDCD.04	IC I⊂ Com
SPDT SWITCH	BGA100PLDCD.05	✓ Cap ✓ Resistor
_01UF_CAP	BGA100PLDCD.06	Connector
_1UF_CAP	BGA100PLDCU.04 BGA100PLDCU.05	Diode
	BGA100PLDCU.06	✓ Transistor
	BGA100PLD0B.05 BGA100PLD0B.06	🔽 Test Point
	BGA1024PLD0B.05	🔽 Transforme
	BGA1089PCD.05	Inductor
	BGA1089PCD.06 BGA1089PCU.05	🗹 Regulator
	BGA1089PCU.06	Other
4 Leads	100 Leads	Next
	Leads are under component	
Leads are on 2 sides		Auto Search
	Horizontal pitch is .059055	
Vertical pitch is 0.1000000	Vertical pitch is .059055	
	0000000000	
	0000000000	
	0000000000	
	0000000000	
	000000000	
	0000000000	





Other features that can be added

- Thermal Contact Board attachment to chassis
- Stiffener Add rigidity to the PCB as well as heat transfer
- Surface Heat Spread heat over part of the board
- Cutout Add a hole or a cutout to the board
- Layer Plate Add metal to the surface or internal to the board to enhance heat transfer

	Add Thermal Contac	t					
	Center Location	Contact Side					
	Add Stiffener						
	Side	~ —	пк				
dd Si	urface Heat Load						
	enter Location	@ Destander	0K				
4	Add Cutout						
	Center Location	 Rectangular Circular 	OK Add				
	Y	C Diagonal points					
	Place with mouse	C Multiple points	Cancel				
		Width	Select points				
	Side C Front		Help				
Add	I Layer Plate						
	Center Location	Rectangular	ОК				
		C Circular	Add				
	Y	Width					
	Place with mouse		Cancel				
		Length	Help				
	% Coverage						
	100.0	Diameter					
L	ayer						
Γ	1 TOP 💌						





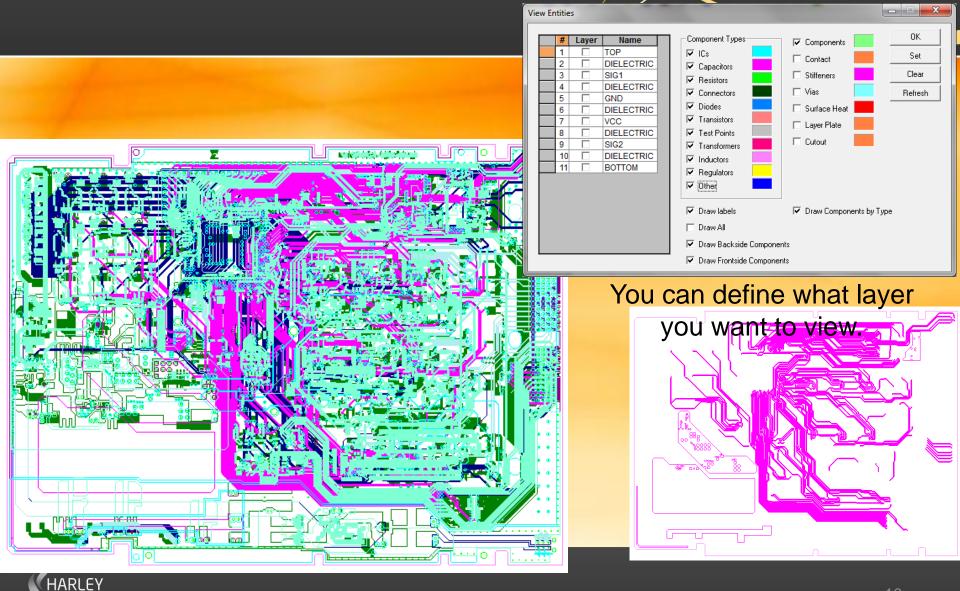
Other features that can be added

- Vias In addition to those imported, thermal vias can be added to help heat transfer into the board.
- Air Flow Cooling air flowing over the board can be simulated.
- Wedgelocks Provide edge cooling.

	Add Vias			
	C Unfilled .00	ing Thickness	# Connected 1 - 3 - 5 - 7 -	Name OK TOP
Si	mple Air Flow Inlet Temperature 35 Flow Width (above PC 0.25		Flow Direction C Left to Right C Right to Left C Bottom to Top C Top to Bottom	CK Add Help Flow Exists
Vedgelock Edge Contact				
	ge temperature	PCB Side C Front I Back		OK Help
Right Edge Tempera Top 0 Bottom 0		ock width		
0 Extension Width 0 Wedgelock Width	Extension v	vidth 🗲	→ Thermal	Contact
0 Wedgelock Length 0 Distance from left/bot 3D Layer If Plate	^{ottom} Top View	,		ock Length e from left/bottom



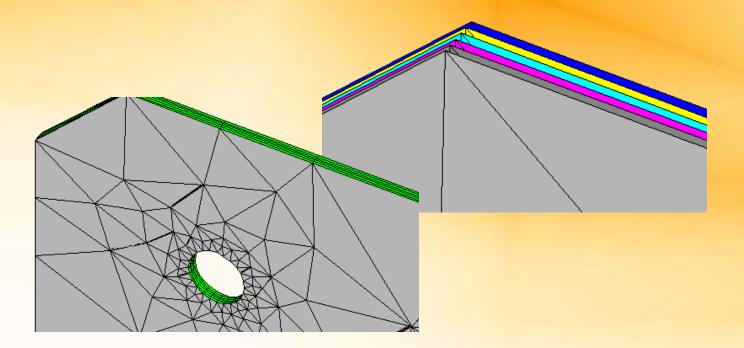
The user can define what they want to see





PCB Automatic Model Generation

- A full 3D model of the PCB is automatically generated.
- The dielectric layers are 3D solid elements
- 2D Plate elements represent metal layers IF ECAD data is NOT imported.

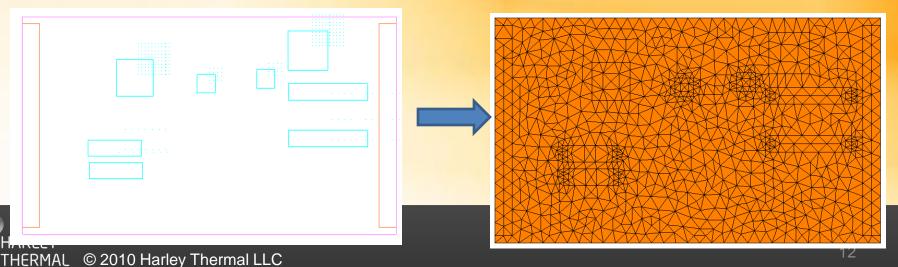






Trace representation in Solaria PCB

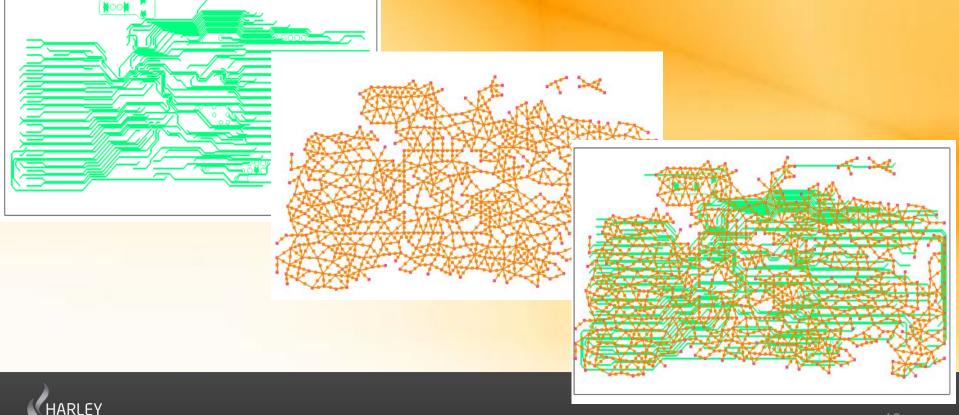
- The board is first meshed exactly representing the PCB outline, components, stiffeners, thermal contact areas, surface heat loads and other geometry. Traces and vias do not influence the mesh. The user can define a general mesh size constraint.
- After the board is meshed, for each metal layer, the traces crossing each triangle in the mesh is thermally represented by three resistors. The metal layer thickness, material and the width of every trace is used in the calculations. This methodology gives an accurate trace representation yet solution times are in minutes.





Trace representation in Solaria PCB

The left picture below shows traces. The middle picture shows the thermal resistors that represent them. The right picture shows them overlaid.





Via representation in Solaria PCB

• The location and diameter of every via is imported. The via plating thickness and material and whether the via is filled or not is defined by the user.

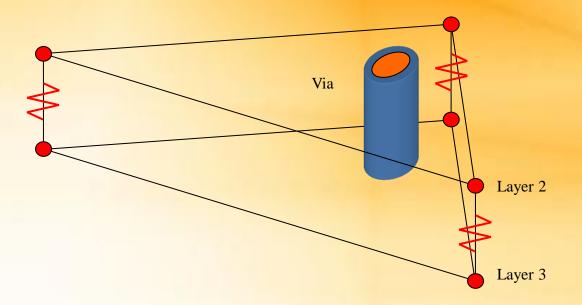
PCB Settings	
General Vias Thermal Geometry Model	
	ОК
Via plating thickness .0014	Cancel
Via drill diameter .02	
Plating material	
Copper	
Fill material	
G-10 EPOXY/GLASS LAMIN/	





Via representation in Solaria PCB

 For each via, the software determines which meshed triangle it lies within. From the ECAD file, the layers the via is electrically connected to is known. Using this information, thermal resistors connecting the nodes on the connected layers are generated.

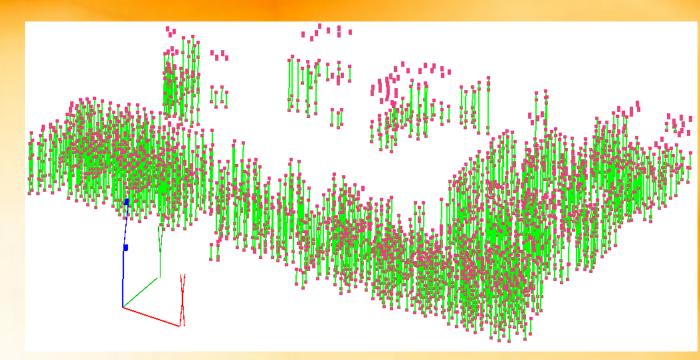




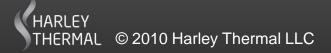


Via representation in Solaria PCB

Via representation, 1041 vias



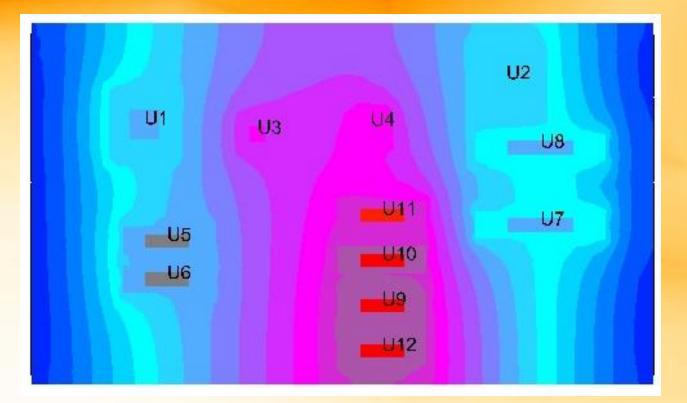
Red dots are nodes, green lines are resistors View has been stretched in the Z direction to better show the resistors.





Post processing Needed

• View component Junction temperatures







Post processing Needed

						SolariaPCB Result	s Summary	29.1	-	_		
	oular sumi operatures		f com	poner	nt	U2 BGA U3 BGA U4 BGA U5 DIP1 U6 DIP1 U7 DIP2	e Pri 100PCD.05 2 100PLDCD.05 1 16PCD.06 2 16PCD.06 2 6P.3W 1 6P.3W 1 4PSB.3W 5 4PSB.3W 5	92.85 113.98 107.38 145.88 144.67	98.76 90.85 111.58 104.98 90.87 89.67 78.01	30ard Ai 98.62 90.92 111.01 104.59 91.16 89.8 76.82 81.89	r C-B Res .02 .13 .13 .9 .9 .6 .6	Cancel Help 1 PCB2 V 1 PCB2 2 PCB3 3 Board1
	nat <u>V</u> iew <u>H</u> elp							1				4 PCB2 5 PCB3
Diffe Coll Coll Board name= RefDes U1 U2 U3 U4 U5 U6 U7 U8 Board name= RefDes U1 U2 U3 U4 U5 U6 U7 U8 Board name= RefDes U1 U2 U3 U4 U5 U6 U7 U8 U9 U7 U8 U9 U10 U11 U12 Board name= Board name= Ref	PCB2 Name Dissipa BGA100PCD.05 2 BGA10PCD.05 2 BGA16PCD.06 2 BGA16PCD.06 2 DIP16P.3W 1 DIP16P.3W 1 DIP24PSB.3W .5 DIP24PSB.3W .5 PCB3 Name Dissipa BGA100PCD.05 2.1 BGA16PCD.06 2 BGA16PCD.06 2 BGA16PCD.06 2 BGA16PCD.06 2 DIP16P.3W 1 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP24PSB.3W .5 DIP16P.3W 2.3 DIP16P.3W 2.3 DIP16P.3W 2.3	$103.36 \\ 1 \\ 113.98 \\ 107.38 \\ 145.88 \\ 144.67 \\ 89.01 \\ 94.61$	Case 98.76 92.85 111.58 104.98 90.87 89.67 78.01 83.61 Case 110.51 110.84 141.24 145.79 115.45 114.77 103.08 101.63 158.05 155.3 150.44 158.35	Board 98.62 90.85 111.01 104.59 91.16 89.8 76.82 81.89 Board 110.27 108.84 140.54 140.54 145.51 116.77 115.75 100.04 98.88 155.43 152.25 146.96 156.11	Air 0 90.92 0 0 0 0 0 0 108.9 0 0 0 0 0 0 0 0 0 0 0 0 0	Case to Board 1 .02 0 .13 .9 .9 .6 .6 .6 .6 .6 .02 0 .13 .13 .9 .6 .6 .6 .6 .6 .6 .9 .9 .9 .9 .9	. 02					C Davd1
RefDes U2 U3 C2 C3 C4 C5 C7 C8 C9 C1 C10 R1 JTAG J4 F1 D1 S1 J7 S1 J7 R0 R2 Board name= RefDes	Name Dissipa EPM72565_7 5.6 74ALS08 1.2 _1UF_CAP 0 _1UF_CAP 0 _1UF_CAP 0 _1UF_CAP 0 _01UF_CAP 0 _00LD_E 0 _00LD_E 0 _00LD_E	258.89 232.08 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Case 246.01 226.68 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Board 246.01 226.66 243.99 242.98 217.39 246 244.88 237.56 209.13 0 240.23 176.14 242.45 204.62 238.25 120.59 88.57 154.61 242.23 242.23 242.51 184.7 179.66 Board	Air 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Case to Board 1 0 .1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0						
	BGA100PCD.05 2 BGA100PLDCD.05	154.36 1	149.76 143.85	149.62 141.85	0 141.92	.02 0	.02					18



Summary

- The ODB++ interface is seamless, simple and fast.
- Every trace, via, component and layer is imported.
- The board mesh is not influenced by the traces or vias but every trace and every via is thermally represented at the meshed triangle level.
- Traces and vias may add tens of thousands of thermal resistors to the model but they are in parallel to those representing the dielectric so the thermal model in the solution is no larger.
- The resulting thermal model is 3D yet solves in minutes.





Summary

- This model has five boards that were generated by SolariaPCB and air flow along the side walls.
- It solved in 12 seconds using the Solaria GCG solver.

